Design of a low-voltage RRIO Fully-Differential two-Stage Op-Amp

Objectives:
1. Understand challenges and constraints imposed by reduced supply voltage.
2. Gain experience in designing for rail to rail input common mode range and rail to rail differential output voltage swing.
3. Gain experience in using dynamic biasing to improve performance via common-mode or large transient sensing.
4. Explore gain enhancement, compensation, and common mode feedback techniques for low voltage applications.
5. Gain experience in layout against gradient errors.
7. Gain experience in current mirror biasing circuit design for improved insensitivity against PVT variations.
8. Validating op amp performance against PVT and ICM variations.

Key Design Tasks:
Design your fully differential two-stage Op Amp, including:
   a. Low voltage band-gap reference circuit that generates a reference current that is insensitive to VDD and temperature variations.
   b. Biasing circuits for your amplifier and CMFB circuit so that the current in any branch consuming 10% or more of the overall current is robust against PVT variations.
   c. Differential input stage with rail-to-rail input common mode range and input gm that varies <= +10% over ICMR over required VDD range.
   d. Input tail current biasing to achieve constant gm with respect to temperature.
   e. Differential output stage with rail-to-rail signal swing and transient output current significantly larger than quiescent current.
   f. Compensation network, CMFB circuit, and gain enhancement.
   g. Sensing and control circuits for dynamic biasing for RR input and large slew rate.

Op Amp Basic Specification Targets:
1. Power supply nominal voltage: VDD = 2.5V, VSS=0V.
   a. Tolerance to voltages down to VDD=2V required (down to VDD=1.5V optional)
   b. Tolerance to voltages up to VDD=5V required.
2. Total current consumption of chip: <= 1 mA at quiescent, targeting <= 0.5mA.
3. Output driving capability: a capacitive load of 5 pF at each output node.
4. Open-loop gain bandwidth (A(s) only) product: >= 50 MHz. (don’t over design)
5. At Q-point with Vicum = 0.5 VDD, DC gain: >= 110dB
   a. At VDD < 2.5 V, DC gain can drop
6. In gain of -1 configuration, 0.1 V step response has overshoot <= 15% over full PVT and ICMR.
7. Settling time in 0.1 V step response in gain of -1: <= 50 ns for +/- 0.001% settling.
8. Differential Vout swing range: VSS to VDD.
9. Input common mode range: VSS to VDD.
10. Slew rate: >= 100 V/μS for both Vo+ and Vo-, >= 200 V/μS for differential output.
11. Output quiescent point errors (deviation from VoQ, which could be defined internally or by the op-amp user externally) should be \( \leq 50 \text{ mV} \) over PVT and ICMR.

12.